

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A method of communicating across a distributed multiprocessing system having a first node with a first processor and a first real memory location and a second node with a second processor and a second real memory location, the first and second nodes ~~processors-being~~ are connected to a central signal routing hub by first and second communication links, respectively, said method comprising the steps of;

indexing the first and second nodes ~~processors~~ to define different destination addresses for each of the nodes ~~processors~~;

processing information within ~~at least one of the first processor of the first node and second processors~~;

addressing the processed information using at least one of the destination addresses;

transmitting the processed information from ~~at least one of the first processor of the first node and second processors~~ across ~~at least one of the first~~ communication link ~~links~~ toward the hub without storing the processed information in the first real memory location of the first node, thereby defining ~~at least one a sending node processor~~;

receiving the processed information along with the ~~at least one~~ destination address within the hub;

identifying the destination ~~of the~~ address for the transmitted processed information within the hub; [[and]]

sending the processed information without modification from the hub over at least one of the communication links to at least one of the first and second nodes ~~processors~~ associated with the ~~at least one~~ destination address, thereby defining at least one addressed node processor; and

storing the processed information within the real memory location of the addressed node.

2. **(Currently Amended)** A method as set forth in claim 1 wherein the step of processing information is further defined as creating data within ~~at least one of the~~ first processor ~~and second processors~~.

3. **(Currently Amended)** A method as set forth in claim 2 wherein the step of processing information is further defined as compiling the data within ~~at least one of the~~ first processor ~~and second processors~~.

4. **(Currently Amended)** A method as set forth in claim 2 wherein the step of transmitting the processed information is further defined as transmitting data along with executable code from the sending node processor to the addressed node processor.

5. **(Currently Amended)** A method as set forth in claim 3 wherein the step of transmitting the processed information is further defined as transmitting the processed information across ~~at least one of the~~ first communication link ~~links~~ in only one direction from ~~at least one of the first processor and second processors~~ to the hub to define a send-only system.

6. **(Currently Amended)** A method as set forth in claim 5 wherein the step of sending the processed information without modification is further defined as sending the processed information from the hub over at least one of the communication links in only one direction from the hub to at least one of the first and second nodes ~~processors~~ to further define the send-only system.

7. **(Currently Amended)** A method as set forth in claim [3] 1 further including the step of directing the ~~sending~~ first processor to a subsequent task to be performed ~~within the processor~~ while simultaneously sending the processed information across ~~one of the~~ first communication link ~~links~~ to the hub.

8. **(Currently Amended)** A method as set forth in claim 1 wherein the step of indexing the first and second nodes ~~processors~~ is further defined as indexing the nodes ~~processors~~ to define an identifier ~~a different code~~ for each of the nodes ~~processors~~ for differentiating the nodes ~~processors~~.

9. **(Currently Amended)** A method as set forth in claim 8 further including the step of creating a virtual memory map of each of the identifiers ~~codes~~ within each of the first and second nodes ~~processors~~ such that the first and second nodes ~~processors~~ can address and forward processed information to each of the indexed nodes ~~processors~~ within the system.

10. **(Currently Amended)** A method as set forth in claim 9 wherein the step of addressing the processed information is further defined as assigning a destination address onto the processed information corresponding to the identifier ~~indicative of the code~~ of the addressed node ~~processor~~.

Claim 11. **(Cancelled).**

12. **(Currently Amended)** A method as set forth in claim 1 ~~[[11]]~~ wherein the step of addressing the processed information ~~[[is]]~~ further comprises the step of ~~defined as~~ assigning a memory address onto the processed information ~~indicative of the~~ corresponding to a location of the real memory location of the addressed node ~~processor~~.

Claim 13. **(Cancelled).**

14. **(Currently Amended)** A method as set forth in claim 8 further including the step of interconnecting the hub to a second hub, having third and fourth nodes

~~processors~~, by a hub link.

15. **(Original)** A method as set forth in claim 14 further including the step of indexing the hubs to define a master hub and a secondary hub.

16. **(Currently Amended)** A method as set forth in claim 15 further including the step of indexing the first, second, third, and fourth nodes ~~processors~~ in accordance with the master and secondary hub indexes to redefine the identifiers ~~codes~~ for each of the nodes ~~processors~~ such that each of the nodes ~~processors~~ can be differentiated.

17. **(Currently Amended)** A method as set forth in claim 16 further including the step of simultaneously sending the processed information to all of the indexed nodes ~~processors~~ by simultaneously placing the destination addresses of each of the indexed nodes ~~processors~~ onto the sent information.

18. **(Currently Amended)** A method as set forth in claim 17 further including the step of limiting the number of times that the processed information can be sent ~~from~~ from a sending nodes ~~processor~~.

19. (Currently Amended) A distributed multiprocessing system comprising;

a first node and a second node with said nodes being separated from each other,

a first processor disposed within said first node for processing information at ~~a first station~~ and for assigning a first address to a first processed information,

a first real memory location disposed within said first node for storing processed information at said first node,

a second processor disposed within said second node for processing information at ~~a second station~~ and for assigning a second address to a second processed information,

a second real memory location disposed within said second node for storing processed information at said second node,

a central signal routing hub,

an indexer connected to said routing hub for indexing said first and second ~~nodes processors~~ to define different destination addresses for each of said ~~nodes processors~~,

a first communication link interconnecting said ~~first processor~~ first node and said hub for transmitting said first processed information between said first processor of said first node and said hub without storing said processed information within said first real memory location of said first node,

a second communication link interconnecting said ~~second processor~~ second node and said hub for transmitting said second processed information between said second

processor of said second node and said hub without storing said processed information within said second real memory location of said second node,

said central routing hub including a sorter for receiving at least one of said first and second processed information from at least one of said first and second nodes ~~processors~~, thereby defining at least one sending node ~~processor~~, and for associating a destination of at least one of said first and second addresses of said first and second processed information, respectively, with at least one of said destination addresses, and for sending at least one of said first and second processed information without modification from said hub over at least one of said communication links to at least one of said first and second nodes ~~processors~~ associated with said destination address, thereby defining at least one addressed node ~~processor~~, with said first and second real memory locations storing processed information received from said hub.

20. **(Original)** A system as set forth in claim 19 wherein said first communication link includes first incoming and first outgoing transmission lines.

21. **(Original)** A system as set forth in claim 20 wherein said second communication link includes second incoming and second outgoing transmission lines.

22. **(Original)** A system as set forth in claim 21 wherein said first and second incoming transmission lines interconnect said first and second processors, respectively, to said hub for transmitting signals in only one direction from said first and

second processors to said hub to define a send-only system.

23. **(Original)** A system as set forth in claim 22 wherein said first and second outgoing transmission lines interconnect said first and second processors, respectively, to said hub for transmitting signals in only one direction from said hub to said first and second processors to further define said send-only system.

24. **(Original)** A system as set forth in claim 23 wherein said first and second incoming transmission lines and said first and second outgoing transmission lines are unidirectional optical fiber links.

25. **(Currently Amended)** A system as set forth in claim 19 further including at least one actuator connected to at least one of said first and second nodes ~~processors~~, respectively, for performing a testing operation during an operation of said system.

26. **(Original)** A system as set forth in claim 25 wherein said actuator is further defined as servo-hydraulic actuator.

27. **(Currently Amended)** A system as set forth in claim 19 wherein said indexer defines an identifier ~~a different code~~ for each of said nodes ~~processors~~ for differentiating said nodes ~~processors~~.

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28. **(Currently Amended)** A system as set forth in claim 27 wherein said first and second nodes ~~processors~~ each include virtual memory maps of each identifier ~~code~~ such that said first and second processors can address and forward processed information to each of said indexed nodes ~~processors~~ within said system.

29. **(Original)** A system as set forth in claim 28 wherein each of said first and second processors further include a hardware portion for assigning said first and second addresses to said first and second processed information, respectively.

30. **(Currently Amended)** A system as set forth in claim 29 wherein said hardware portion assigns a destination address onto said processed information corresponding to said identifier ~~indicative of said code~~ of said addressed node ~~processor~~.

31. **(Currently Amended)** A system as set forth in claim 30 ~~further including wherein said~~ first real memory location is connected to said hardware portion of said first processor and said second real memory location is connected to said hardware portion of said second processor, ~~said first and second memory locations storing received~~ processed information.

32. **(Currently Amended)** A system as set forth in claim 31 wherein said hardware portion assigns a memory address onto said processed information ~~indicative of an~~ corresponding to a location of an associated first and second real memory location of said

addressed node ~~processor~~.

33. **(Currently Amended)** A system as set forth in claim 27 further including a second hub, having third and fourth nodes ~~processors~~, interconnected to said first hub by a hub link.

34. **(Currently Amended)** A system as set forth in claim 33 wherein said indexer indexes said first and second hubs to define a master hub and secondary hub and indexes said first, second, third, and fourth nodes ~~processors~~ to redefine said identifiers ~~codes~~ for each of said nodes ~~processors~~ for differentiating said nodes ~~processors~~.

35. **(Original)** A system as set forth in claim 34 further including a key disposed within one of said first and second hubs to determine which of said hubs will be defined as said master hub.

36. **(Original)** A system as set forth in claim 19 wherein each of said first and second processors further include at least one task.

37. **(Original)** A system as set forth in claim 36 wherein said processors include executable code for processing information defined by each of said tasks.

38. **(Currently Amended)** A system as set forth in claim 37 wherein said task includes at least a pair of pointers for directing a flow of data from said sending node processor to said destination node processor.

39. **(Currently Amended)** A system as set forth in claim 38 wherein said ~~pair of~~ pointers includes a next task pointer for directing said sending processor to a subsequent task to be performed, and at least one data destination pointer for directing said first and second processor associated with said sending node to send ~~sending~~ said processed information across said first communication link ~~one of said incoming transmission lines~~ to said hub.

40. **(Currently Amended)** A system as set forth in claim 39 wherein said at least one data destination pointer includes a plurality of data destination pointers to direct said first and second processor associated with said sending node to simultaneously forward processed information to a plurality of addressed nodes ~~processors~~.

41. **(Original)** A system as set forth in claim 39 further including a chipset interconnected between each of said incoming and outgoing communication links and said corresponding processors for creating a virtually transparent connection therebetween.

42. **(Original)** A system as set forth in claim 41 further including a buffer disposed between each of said processors and said chipsets.

43. **(Currently Amended)** A system as set forth in claim 42 further including a counter for determining a number of times ~~that said~~ processed information is sent to said addressed node ~~processor~~.

44. **(Original)** A system as set forth in claim 43 further including a sequencer for monitoring and controlling a testing operation as performed by said system.

45. **(Currently Amended)** A system as set forth in claim 19 further including a host computer connected to one of said first and second nodes ~~processors~~, said host computer having a ~~digital signal~~ processing card and at least one peripheral device.

46. **(Original)** A system as set forth in claim 45 wherein said peripheral devices are further defined as a monitor, a printer, a key board, and a mouse.

47. **(Currently Amended)** A system as set forth in claim 19 wherein said sorter includes hardware for determining said destination addresses of said addressed node ~~processors~~.

Claims 48.-67. **(Cancelled)**